256K (32K x 8) Paged CMOS E^2PROM

Features

- **Fast Read Access Time - 150 ns**
- **Automatic Page Write Operation**
  - **Internal Address and Data Latches for 64-Bytes**
  - **Internal Control Timer**
- **Fast Write Cycle Times**
  - **Page Write Cycle Time: 3 ms or 10 ms Maximum**
  - **1 to 64-Byte Page Write Operation**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **200 µA CMOS Standby Current**
- **Hardware and Software Data Protection**
- **$\overline{\text{DATA}}$ Polling for End of Write Detection**
- **High Reliability CMOS Technology**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 Years**
- **Single 5V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

Description

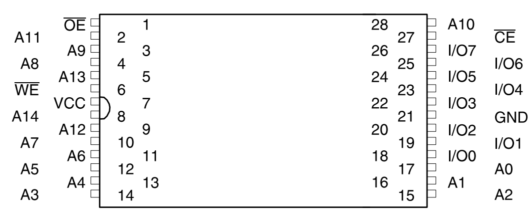
The AT28C256 is a high-performance Electrically Erasable and Programmable Read Only Memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 µA.

(continued)

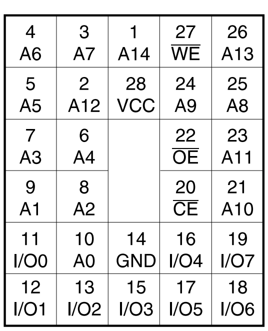
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

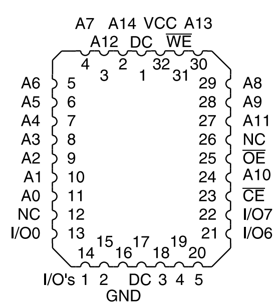
TSOP
Top View



PGA
Top View

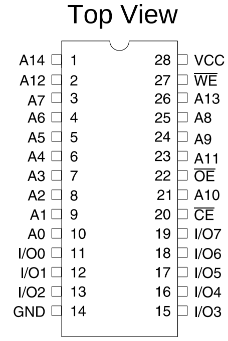


LCC, PLCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

CERDIP, PDIP,
FLATPACK, SOIC
Top View



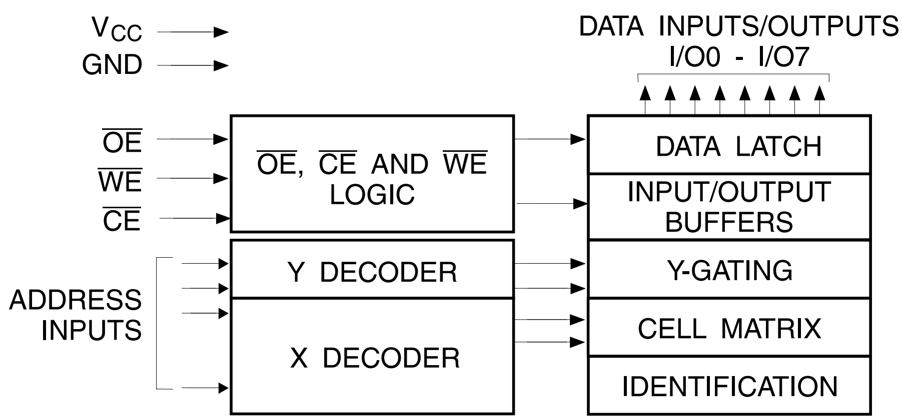
0006F

Description (Continued)

The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64-bytes simultaneously. During a write cycle, the addresses and 1 to 64-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C256 allows 1 to 64-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{\text{DATA}}$ POLLING: The AT28C256 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 64-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.

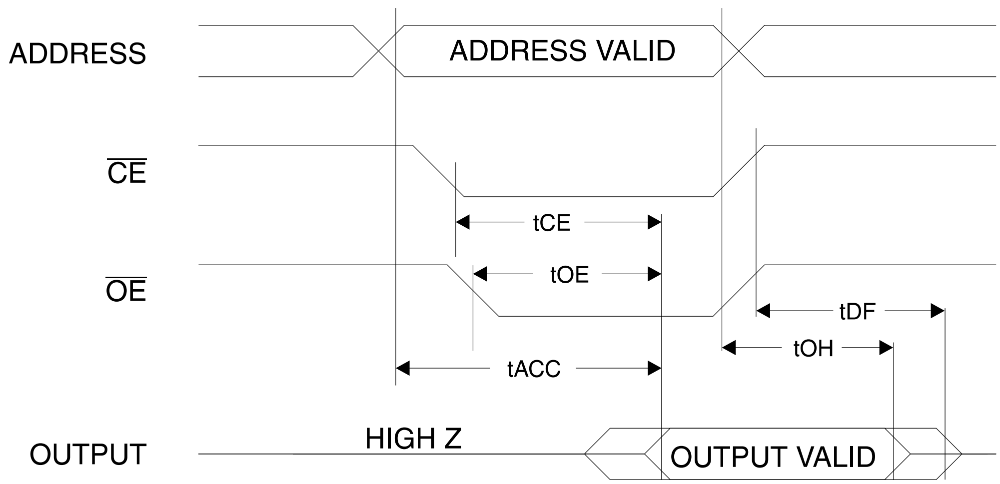
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V	Com., Ind.		200	µA
			Mil.		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V			3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			50	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

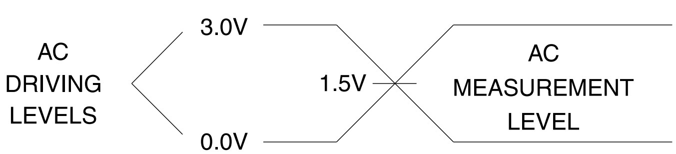
Symbol	Parameter	AT28C256-15 Min	AT28C256-15 Max	AT28C256-20 Min	AT28C256-20 Max	AT28C256-25 Min	AT28C256-25 Max	AT28C256-35 Min	AT28C256-35 Max	Units
t_{ACC}	Address to Output Delay		150		200		250		350	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250		350	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	70	0	80	0	100	0	100	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



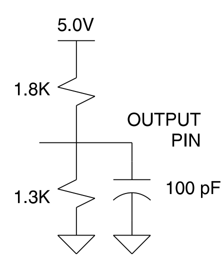
Notes: 1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

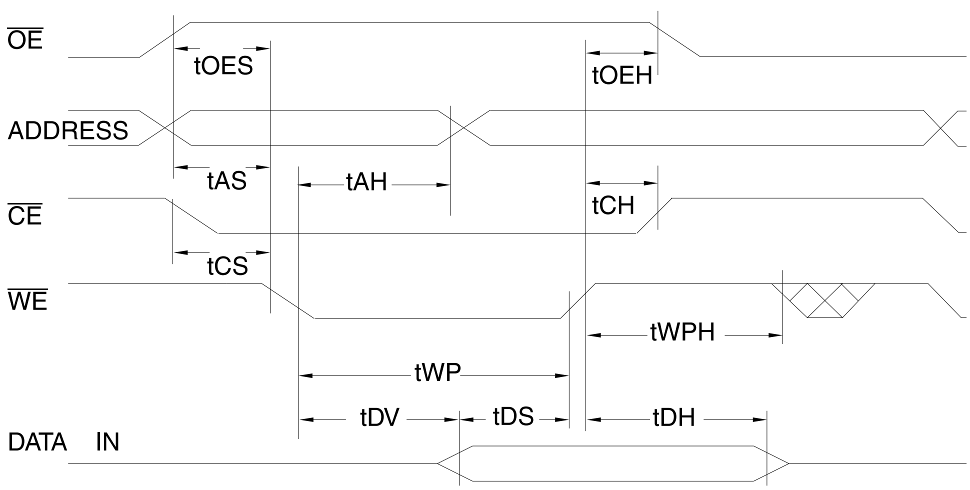
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR (1)		

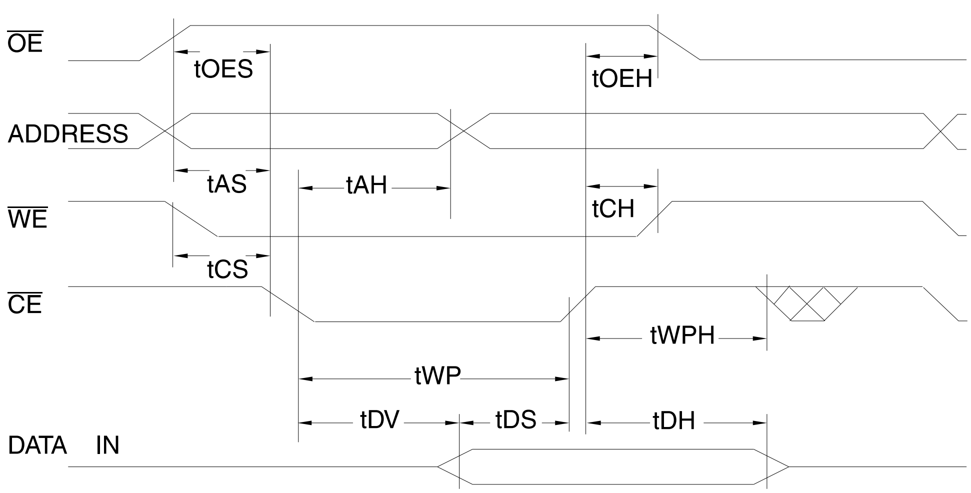
Note: 1. NR = No Restriction

AC Write Waveforms

$\overline{WE}$ Controlled



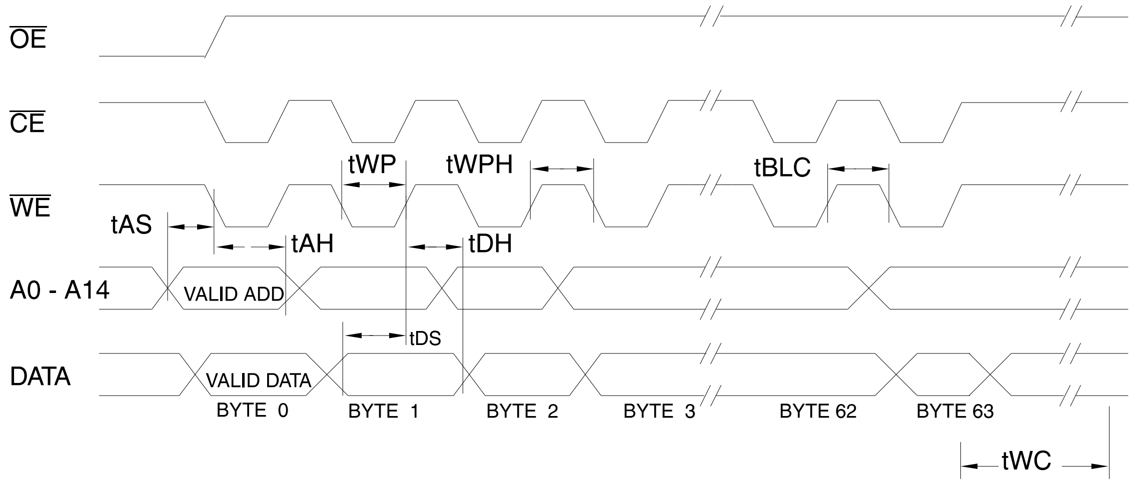
$\overline{CE}$ Controlled



Page Mode Characteristics

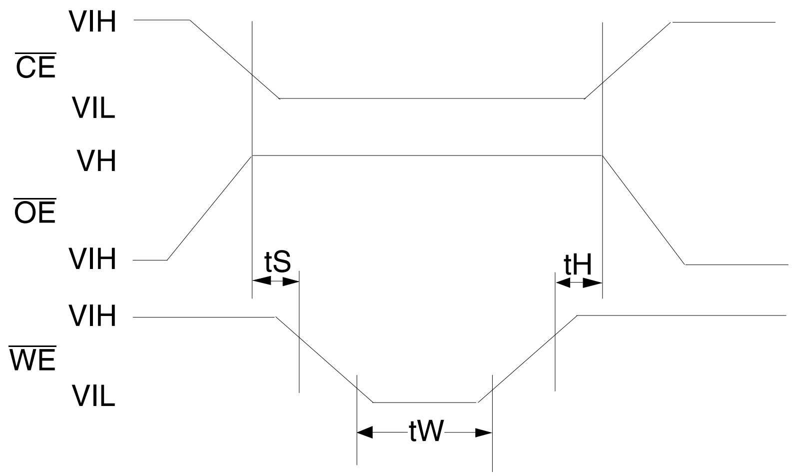
Symbol	Parameter		Min	Max	Units
t_{WC}	Write Cycle Time	AT28C256		10	ms
		AT28C256F		3.0	ms
t_{AS}	Address Set-up Time		0		ns
t_{AH}	Address Hold Time		50		ns
t_{DS}	Data Set-up Time		50		ns
t_{DH}	Data Hold Time		0		ns
t_{WP}	Write Pulse Width		100		ns
t_{BLC}	Byte Load Cycle Time			150	µs
t_{WPH}	Write Pulse Width High		50		ns

Page Mode Write Waveforms (1, 2)



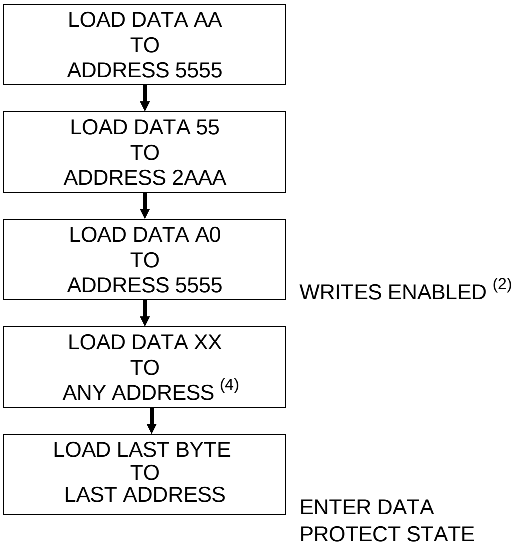
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Chip Erase Waveforms



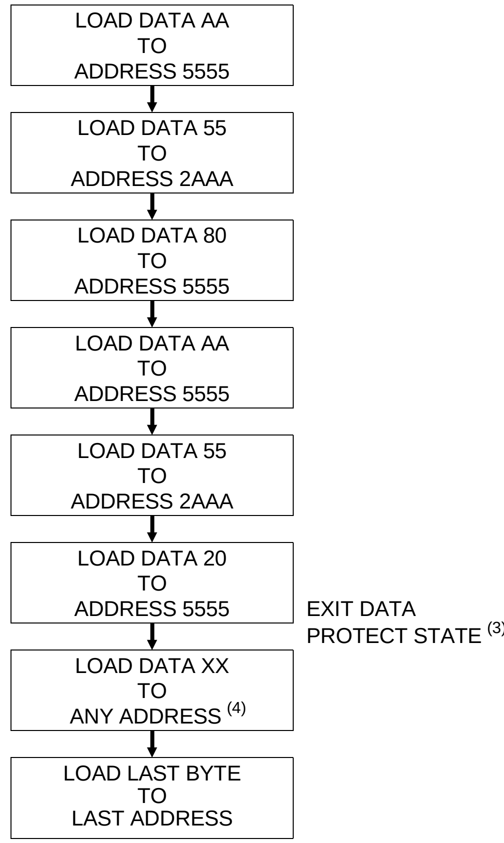
$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm (1)

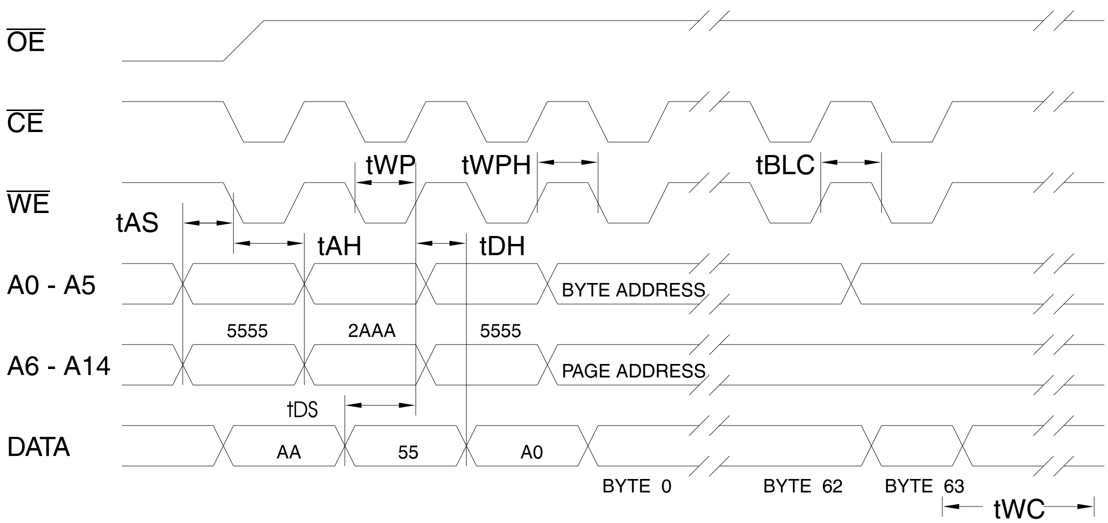


Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64-bytes of data are loaded.

Software Data Protection Disable Algorithm (1)



Software Protected Write Cycle Waveforms (1, 2)



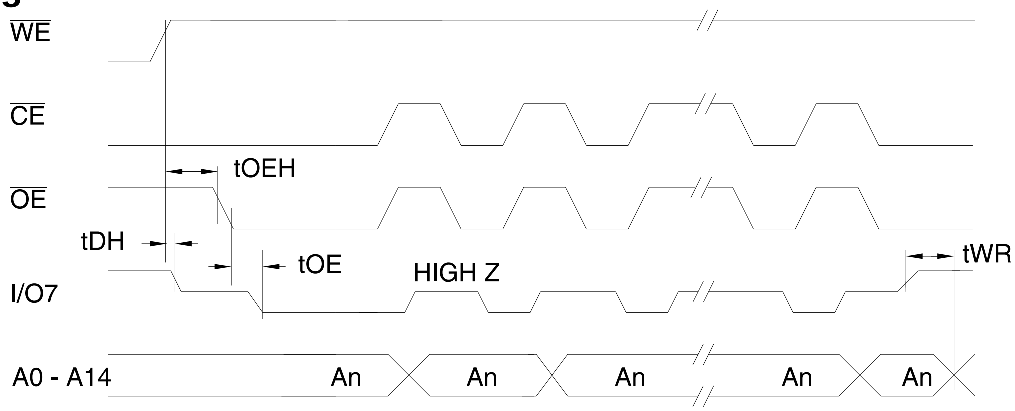
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	OE Hold Time	0			ns
t_{OE}	OE to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Data Polling Waveforms

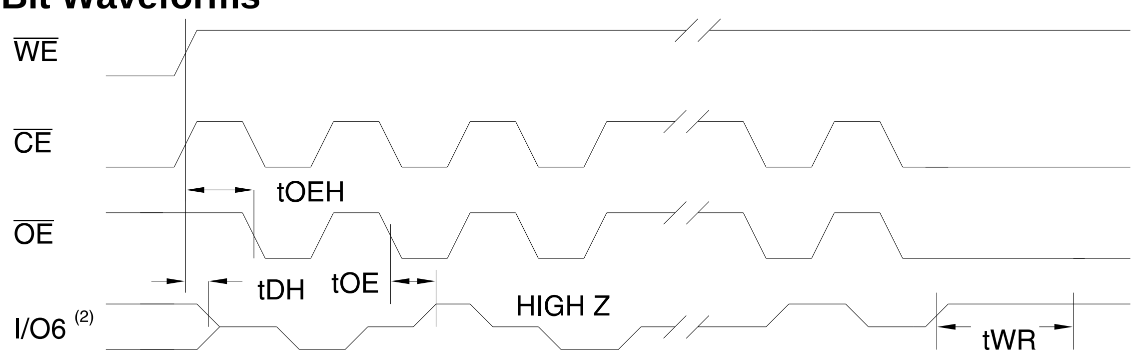


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	OE Hold Time	10			ns
t_{OE}	OE to Output Delay (2)				ns
t_{OEHP}	OE High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

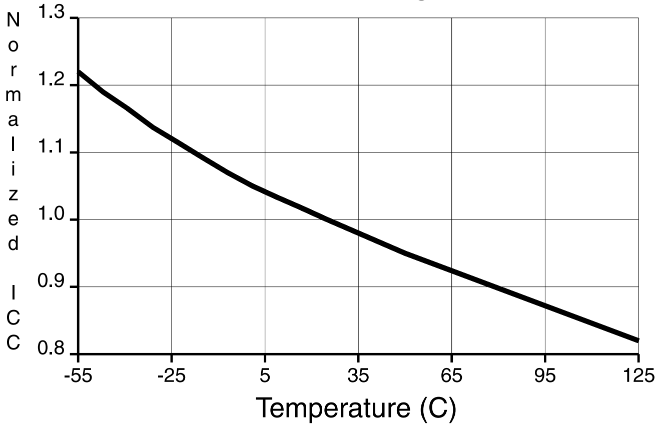
Notes: 1. These parameters are characterized and not 100% tested. 2. See AC Read Characteristics.

Toggle Bit Waveforms (1, 2, 3)

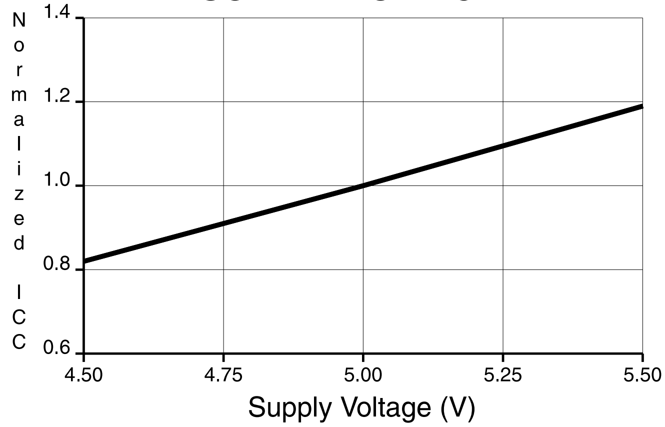


Notes: 1. Toggling either OE or CE or both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

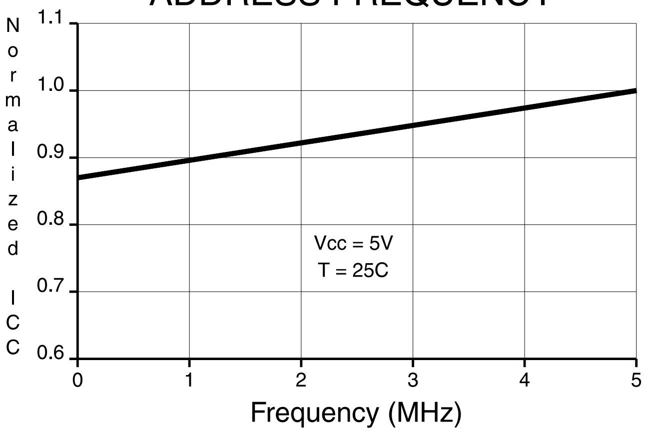
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information [(2)]

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
150	50	0.2	AT28C256(E,F)-15JC AT28C256(E,F)-15PC AT28C256(E,F)-15SC AT28C256(E,F)-15TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C256(E,F)-15JI AT28C256(E,F)-15PI AT28C256(E,F)-15SI AT28C256(E,F)-15TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-15DM/883 AT28C256(E,F)-15FM/883 AT28C256(E,F)-15LM/883 AT28C256(E,F)-15UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	50	0.2	AT28C256(E,F)-20JC AT28C256(E,F)-20PC AT28C256(E,F)-20SC AT28C256(E,F)-20TC	32J 28P6 28S 28T	Commercial (0°C to 70°C)
			AT28C256(E,F)-20JI AT28C256(E,F)-20PI AT28C256(E,F)-20SI AT28C256(E,F)-20TI	32J 28P6 28S 28T	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-20DM/883 AT28C256(E,F)-20FM/883 AT28C256(E,F)-20LM/883 AT28C256(E,F)-20UM/883	28D6 28F 32L 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	50	0.2	AT28C256(E,F)-25JC AT28C256(E,F)-25PC AT28C256-W	32J 28P6 DIE	Commercial (0°C to 70°C)
			AT28C256(E,F)-25JI AT28C256(E,F)-25PI	32J 28P6	Industrial (-40°C to 85°C)
	50	0.3	AT28C256(E,F)-25DM/883 AT28C256(E,F)-25FM/883 AT28C256(E,F)-25LM/883 AT28C256(E,F)-25UM/883 AT28C256(E,F)-35UM/883	28D6 28F 32L 28U 28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.2	AT28C256-W	DIE	Commercial (0°C to 70°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150 (3)	50	0.35	5962-88525 16 UX 5962-88525 16 XX 5962-88525 16 YX 5962-88525 16 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 15 UX 5962-88525 15 XX 5962-88525 15 YX 5962-88525 15 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 14 UX 5962-88525 14 XX 5962-88525 14 YX 5962-88525 14 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 08 UX 5962-88525 08 XX 5962-88525 08 YX 5962-88525 08 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 07 UX 5962-88525 07 XX 5962-88525 07 YX 5962-88525 07 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 06 UX 5962-88525 06 XX 5962-88525 06 YX 5962-88525 06 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200 (3)	50	0.35	5962-88525 12 UX 5962-88525 12 XX 5962-88525 12 YX 5962-88525 12 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 04 UX 5962-88525 04 XX 5962-88525 04 YX 5962-88525 04 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250 (3)	50	0.35	5962-88525 13 UX 5962-88525 13 XX 5962-88525 13 YX 5962-88525 13 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 11 UX 5962-88525 11 XX 5962-88525 11 YX 5962-88525 11 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

(continued)

Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.35	5962-88525 05 UX 5962-88525 05 XX 5962-88525 05 YX 5962-88525 05 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 03 UX 5962-88525 03 XX 5962-88525 03 YX 5962-88525 03 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	50	0.35	5962-88525 10 UX 5962-88525 10 XX 5962-88525 10 YX 5962-88525 10 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 02 UX 5962-88525 02 XX 5962-88525 02 YX 5962-88525 02 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
350	50	0.35	5962-88525 09 UX 5962-88525 09 XX 5962-88525 09 YX 5962-88525 09 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)
	50	0.35	5962-88525 01 UX 5962-88525 01 XX 5962-88525 01 YX 5962-88525 01 ZX	28U 28D6 32L 28F	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Notes: 1. Electrical specifications for these speeds are defined by Standard Microcircuit Drawing 5962-88525.
2. See Valid Part Number table below.
3. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to *every* device type in the SMD is 100% tested for this feature.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C256	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	-	W

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
28F	28 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)
28U	28 Pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms